SESSION 2 – TAPA II
RF Subsystems

Thursday, June 17, 10:20 a.m.
Chairpersons: A. Abidi, UCLA
H. Sato, Renesas

2.1 — 10:20 a.m.

An Integrated 17 GHz Front-End for ISM/WLAN Applications in 0.13 µm CMOS, C. Kienmayer, R. Thüringer, M. Tiebout*, W. Simbürger* and A. L. Scholtz, Technical University of Vienna, *Infineon Technologies AG, Munich, Germany

This paper presents an integrated front-end for ISM/WLAN applications at 17.3GHz in 0.13 µm standard CMOS. The front-end chip includes an inductive source-degenerated low noise amplifier (LNA), a transformer-based Gilbert-mixer, an intermediate frequency (IF) amplifier and a buffer for the local oscillator(LO) input. The integrated receiver front-end achieves a gain of 34.7 dB, a SSB noise figure of 6.6 dB, an input IP3 of -34.4 dBm and an input 1dB compression point of -39 dBm and consumes only 70 mW at a power supply voltage of 1.5 V.

2.2 — 10:45 a.m.

A 72mW CMOS 802.11a Direct Conversion Receiver with 3.5dB NF and 200kHz 1/f Noise Corner, G. Montagna, R. Castello*, R. Tonietto*, M. Valla and I. Bietti, STMicroelectronics, Pavia, Italy, *Università di Pavia, Pavia, Italy

A receiver front-end for 802.11a in 0.13um CMOS operated from 1.2/2.5V has anactive area of 1.8 mm2 and consumes 72mW (half in the receiver path and half in the synthesizer). Overall NF is 3.5 dB with a 1/f noise corner at 200kHz, and an IIP3 of -2dBm. Synthesizer DSB integrated phase noise is-36dBc. The front-end reported here is one of the lowest power consumption and 1/f noise corner in pure CMOS for this application.

2.3 — 11:10 a.m.

An Ultra-Low Power MEMS-Based Two-Channel Transceiver for Wireless Sensor Networks, B.P. Otis, Y.H. Chee, R. Lu, N.M. Pletcher, and J.M. Rabaey, University of California, Berkeley, CA

This paper explores the design and implementation of a low-power two-channel transceiver using micromachined resonators. Wireless sensor networks require transceivers that are small, cheap, and power efficient. RF-MEMS resonators are utilized to accommodate these constraints. The prototype 1.9GHz transceiver, designed in 0.13um CMOS, operates at 1.2V and consumes 3mA in receive mode and transmits 1.6dBm with 17% efficiency. The two 40kb/s channels achieve a sensitivity of –78dBm with a 10us receiver start-up time.

2.4 — 11:35 a.m.

An Injection Locked, RF Powered, Telemetry IC in 0.25µm CMOS, F. Kocer, P.M. Walsh and M.P. Flynn, University of Michigan, Ann Arbor, MI

We present a new architecture for efficient power transfer increasing the operational range of a batteryless wireless transponder. A new, very low-powerclock extraction technique based on injection locking is used to generate a low phase noise system clock. This generates a very low phase noise 900MHz clock locking onto a super-harmonic or sub-harmonic incident RF signal. A continuous wave (CW) modulation technique is employed for data transmission for its simplicity and low power consumption.